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SDR Applications using VLSI Design of Reconfigurable Devices

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ABSTRACT

The design of future multi-standard systems is very challenging. Flexible architectures exploiting processing commonalities of the different set of standard scohabiting in the device offer promising solutions. This paper presents a graphical approach for the optimization of multi-standard Software Defined Radio(SDR) systems. The potential of our approach for optimizing multi-standard SDR systems is highlighted by considering a realistic example of channelizers for SDR systems. In this paper we compare several channelization techniques. Computational complexity for multi-standards, multi-channels channelizers is presented that is to be included for the optimization procedure of flexible systems. Results show that Frequency Response Masking(FRM) technique is most suitable as compared to others.

Keywords : Coefficient Decimation Method, Low Complexity, Reconfigurability, FIR Channel Filter

I. INTRODUCTION

Software defined radios (SDR) can significantly reduce the cost and complexity of today„s cellular radio base stations. Software radios architectures centre on the use of wide band (WB) A/Dconverters and D/A converters as close to the antenna as possible, with as much radio functionality as possible implemented in the digital domain. The reconfigurable FIR filters are widely used in multiband mobile communication system. The filters using in mobile communication system must be operating in low frequency and realize to consumes lesspowerandhighspeed.Theadvancetechnologies in mobile communication systems are demanding the low power and low complexity techniques. The Software Defined Radio (SDR) and the FIR filter researches are focused on reconfigurable realizations [2]. The SDR technology used to replace the analog signal processing with digital signal processing in order to provide flexible reconfiguration. A SDR design must meet today'sreconfigurability requirements and adapt to emerging standards, as well as accommodate cost, power and performance demands. Reconfigurability of the receiver to work with different wireless communication standards is another key requirement in an SDR. Generally the complexity of FIR filter depends upon the number of adders performs in the multiplier unit. Channelizers is known as the most important block of the SDR which operates in high sampling rate but the SDR mustberealizingoflowpowerconsumptionandhigh speed. Using a bank of FIR filters in the channel filters introduces the multiple numbers of narrowband channels from a wideband signal. Software defined radio (SDR) is one of the most important topics of research, and indeed development, in the area of mobile and personal communications. SDR is viewed as an enabler of global roaming and as a unique platform for the rapid introduction of new services into existing live networks. It therefore promises mobile communication networks a major increase in flexibility and capability [1]. SDR is defined as aradio

in which the receive digitization is performed atsome stage downstream from the antenna, typically after wideband filtering, lownoise amplification, and down conversiontoalowerfrequencyinsubsequentstages- with a reverse process occurring for the transmit digitization. Digital signal processing in flexible and reconfigurable functional blocks defines the characteristicsoftheradio[2].DesignofSDRsystems is very challenging because it is very difficult to designasystemthatpreservesmostoftheproperties of the ideal software radio while being realizable with current-day technology. The possibilities to design software radio architectures range from "Velcro" approach to a "Very Fine Grain" approach [3]. The "Velcro" approach aims to support several communication standards through a few self-contained complex communication components;each exclusively dedicated to a given standard. On the contrary, "Very Fine Grain" approach is based on manipulating small size operators/components to support differentstandards.

II. LITERATURESURVEY

ThePCapproachisastraightforwardapproachan d hence relatively simple. But the main drawbackis that,thenumberofbranchesoffiltering-DDC-SRC is directly proportional to the numberof received channelsi,e.ThecomplexityofthePCapproachis directly proportional to the number of channels. Hence the PC approach is not efficient whenthe number of received channels is large. The filters used in the PC approach are of a very highorder andtheseresultsinhighareacomplexityandthus increased static power. DFTFBs cannot extract channels with different bandwidths known as nonuniformchannels,becausetheyaremodulate d FBswithequalbandwidthforallbandpassfilters– the bandwidthsaresameasthatoftheprototypeLPF. Therefore, for multi-mode receivers, distinct DFTFBs are required for each communication standard.Hencethecomplexitythechannelizer increaseslinearlywiththenumberofstandards.If thechannelbandwidthisverysmallcomparedwith wideband input signal (extremely narrowband channels), the prototype filter must behighly selectiveresultinginaveryhigh-orderfilter.Asthe order of the filter increases, the complexity increases linearly. Also the DFT size needs to be increased. Pucker, L. in paper [2] entitled — Channelization techniques for software defined radio‖proposedDFTFilterBanks.DFTfilterbankis auniformlymodulatedfilterbank,whichhasbeen developedasanefficientsubstituteforPCapproach whenthenumberofchannelsneedtobeextracted ismore,andthechannelsareofuniformbandwidth (forexamplemanysinglestandardcommunicatio n channelsneedtobeextracted).Themainadvantage of DFT filter bank is that, it can efficiently utilize the polyphone decomposition of filters. The limitations of DFTFBs are that the channel filters havefixedequalbandwidthscorrespondingtothe specificationofagivenstandard"s.MAHESHet.al. in paper [3] entitled — Reconfigurable Low Area Complexity Filter Bank Architecture Based on Frequency Response Masking for Non uniform Channelization in Software Radio Receivers‖ proposed a new reconfigurable FB based on the FRMapproachforextractingmultiplechannelsof non uniform bandwidths. The FRM approach is modified to achieve following advantages: 1) incorporatereconfigurabilityatthefilterleveland architecturallevel,2)improvethespeedoffiltering operation,and3)reducethecomplexity.

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III. FIR FILTER WITH MULTIPLIERBLOCK

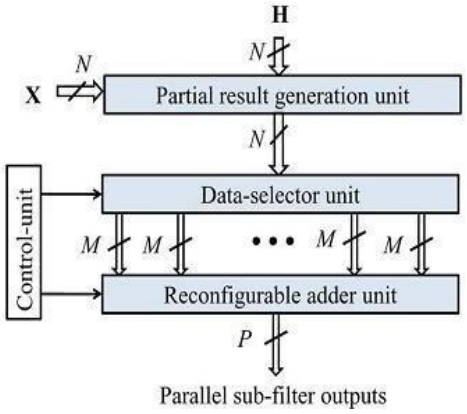

Figure 1. Full parallel reconfigurable filter structure where partial results are shared for interpolation filter.

Figure 1 shows three full-parallel, fixed-coefficient FIR filter structures that are mathematically identical but differ in architecture. Derived from the standard FIR structure using cut-set retiming, the transposed FIR yields an identical mathematical response but with several advantages for FPGA implementation:

1. No input sample shift registers are required since each sample is fed to each tap simultaneously
2. Thepipelinedadditionchainmapsefficiently
3. Filter latency isreduced
4. Identical tap coefficient magnitudes canshare multiplication hardware because taps receive the input samplesimultaneously.

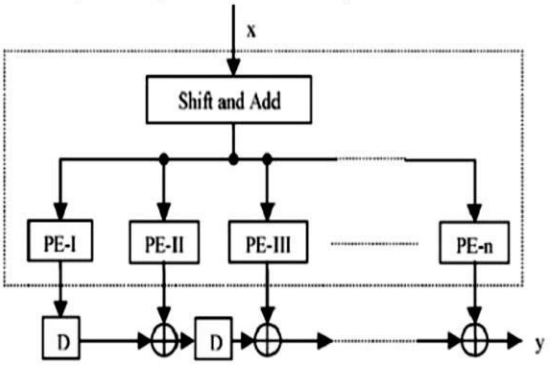

Figure 2. Transposed direct form of an FIR filter

In the transposed direct form, the coefficient multipliers (shown as dotted outline in Figure-1) share the same input and hence commonly known as Multiplier Block (MB). The Multiplier Block (MB) reduces the complexity of the FIR filter implementations, by exploiting the redundancy in MCM. Thus, redundant computations (partial product additions in the multiplier) are eliminated usingBCSE.TheBCSEmethodinwasformulatedas a low complexity solution to realize application specific filters where the coefficients are fixed. In the case of channel filters for Software Defined Radio (SDR) receivers, the coefficients need to be changed as the filter specification changes with the communication standard.

Therefore, reconfigurability is a necessary requirement for Software Defined Radio (SDR) channel filters. In thenextsection,weproposetwoarchitecturesthat incorporate reconfigurability into the BCSE-based low complexity filter architecture. Although we use BCSE to illustrate proposed reconfigurable filter architectures.

IV. PROPOSED FILTERARCHITECTURES

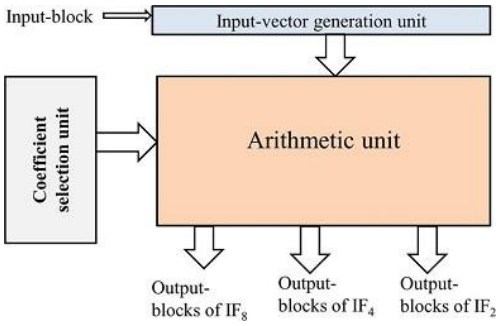

Figure3. Proposedreconfigurablearchitecturefora setofinterpolationfiltersofup-samplingfactors

Inthissection,thearchitectureoftheproposedFIR filter is presented. Our architecture is based on the transposed direct form FIR filter structure asshown in Figure 2. The dotted portion in Figure 1 represents the MB. In Figure 3, PE-i represents the processing element corresponding to theith

coefficient. PE performs the coefficient multiplication operation with the help of a shift and add unit which will be explained in the latter part of this section. The architecture of PE is different for proposed MSG and PSM. In the MSG, the filter coefficients are partitioned into fixed groups and hence the PE architecture involves constant shifters. But in the PSM, the PE consists of programmable shifters (PS). The functions of different blocks of the PE are illustrated below.

Shift and Add Unit:

It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize it using shift and add operations. In contrast to conventional shift and add units used in previously proposed reconfigurable filter architectures, we use the BCSs-based shift andadd unit in our pro-posed MSG and PSM architectures. The architecture of shift and add unit is shown in Figure-3.Theshiftandaddunitisusedtorealizeall the 3-bit BCSs of the input signal ranging from [00 0] to [1 1 1]. In Figure-3, "x >>k" represents the input x shifted right by k units. All the3-bit BCSs [0 1 1], [1 0 1], [1 1 0], and [1 1 1] of a 3-bit number are generated using only three adders, whereas a conventional shift and add unit would require five adders. Since the shifts to obtain the BCSs are known beforehand, PS is not required. All these eight BCSs (including [000]) are then fed to the multiplexer unit. In both the architectures (MSGand PSM) proposed in this paper, we use the sameshiftandaddunit.Thus,theuseof3-bitBCSs reducesthenumberofaddersneededtoimplement the shift and add unit compared to conventional shift and addunits.

Multiplexer Unit:

The multiplexer units are used to select the appropriateoutputfromtheshiftandaddunit.All themultiplexerswillsharetheoutputsoftheshift andaddunit.Theinputstothemultiplexersarethe 8/4 inputs from the shift and add unit and hence 8:1/4:1 multiplexer units are employed in the architecture. The select signals of the multiplexers are the filter coefficients which are previously stored in a look up table (LUT). The MSG and PSM architectures basically differ in the way filter coefficients are stored in the LUT. In the MSG, the coefficients are directly stored in LUTs without any modification whereas in PSM, the coefficients are stored in a coded format. The number of multiplexers will also be different for PSM and MSG. In MSG, the number of multiplexers will be dependent on the number of groups after the partitioning of the filter coefficient into fixed groups. The number of multiplexers in the PSM is dependent on the number of non-zero operands in the coefficient for the worst case after the application of BCSE algorithm.

Final Shifter Unit

The final shifter unit will perform the shifting operation after all the intermediate additions(i.e., intra-coefficient additions) are done. This can be illustratedusingtheoutputexpressionshiftandadd unitisshowninFigure-3.Theshiftandaddunitis usedtorealizeallthe3-bitBCSsoftheinputsignal rangingfrom[000]to[111].InFigure-3,"x>>k" represents the input x shifted right by k units. All the3-bitBCSs[011],[101],[110],and[111]ofa 3-bitnumber are generated using only threeadders, whereas a conventional shift and add unit would require five adders. Since the shifts to obtain the BCSsareknownbeforehand,PSisnotrequired.All theseeightBCSs(including[000])arethenfedto the multiplexer unit. In both the architectures (MSGandPSM)proposedinthispaper,weusethe sameshiftandaddunit.Thus,theuseof3-bitBCSs reducesthenumberofaddersneededtoimplement the shift and add unit compared to conventional shift and addunits.

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Final Adder Unit:

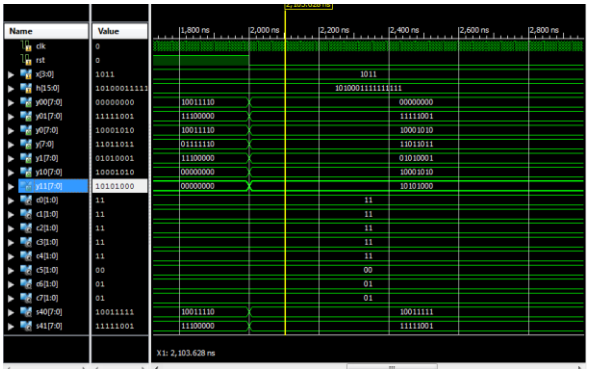
This unit will compute the sum of all the intermediate additions 2−4(x +2−2x) and 2−15(x +2−1x) as in [2]. As the filter specifications of different communication standards are different, the coefficients change with the standards. In conventional reconfigurable filters, the new coefficient set corresponding to the filter specificationofthenewcommunicationstandardis loadedintheLUT.Subsequently,theshiftandadd unit performs a bitwise addition afterappropriate shifts. On the contrary, the proposed PSM architectures perform a binary common sub expression (BCS)-wise addition (instead bitwise addition). Thus, the same hardware architecture can be used for different filter specifications to achievethenecessaryreconfigurability.Moreover, theproposedBCSbasedshiftandaddunitreduces addition operations and hence offers hardware complexityreduction.Architecturecanbeusedfor different filter specifications to achieve the necessaryreconfigurability.

Moreover, the proposed BCS-based shift and add unit reduces addition operations and hence offers hardware complexity reduction.

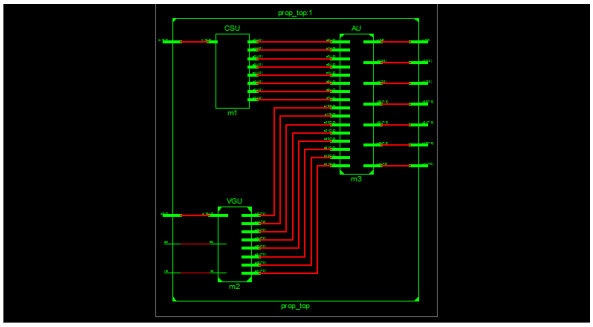
V. SIMULATIONRESULTS

The written Verilog HDL Modules have successfully simulated and verified using Modelsim6.4b and synthesized using Xilinxise13.2.

Top Module 16 bit Interpolation Filter:

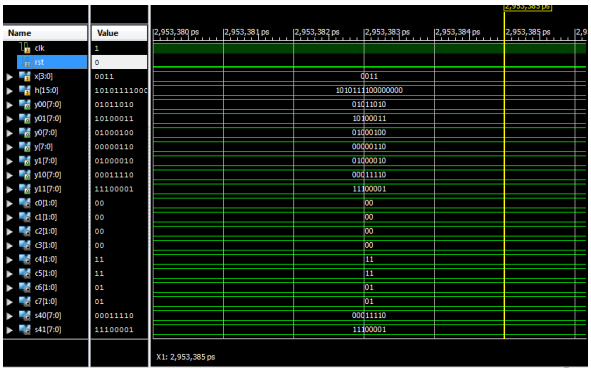


RTL Schematic:

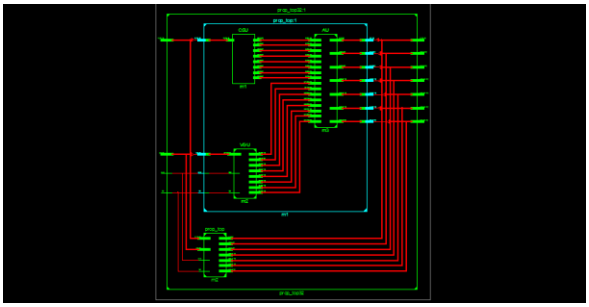


Extension Work:

The proposed system can be done using Dadda multiplier, by using this delay will be reduced.



RTL Schematic:



VI. CONCULSION

The proposed reconfigurable filters architecture results in low area and low delay. The FRM reconfigurabletechniqueismodifiedtoimprovethe speed and reduce the complexity. Synthesis results showthattheproposedFBoffersareareduction.

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